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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/872,924	06/01/2001	James J. deBlanc	10007686-1	3268

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HEWLETT-PACKARD COMPANY
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EXAMINER

LEE, CHRISTOPHER E

ART UNIT	PAPER NUMBER
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2112

DATE MAILED: 04/13/2004

8

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/872,924

Applicant(s)

DEBLANC ET AL.

Examiner

Christopher E. Lee

Art Unit

2112

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 22 March 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-5,7,9-18 and 20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 1-3,5,7 and 11 is/are allowed.
- 6) ☒ Claim(s) 4,9,10,12-18 and 20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 22 March 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 2.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Receipt Acknowledgement

1. Receipt is acknowledged of the Amendment filed on 22nd of March 2004. Claims 1, 3-5, 7, 12, and 14-17 have been amended; claims 6, 8 and 19 have been canceled; and no claim has been newly added since the Non-Final Office Action was mailed on 17th of December 2003. Currently, claims 1-5, 7, 9-18 and 20 are pending in this application.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claim 10 is rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for achieving sufficient isolation by active circuitry instead of passive components (i.e., alternatively; See Application, page 11, lines 20-27), does not reasonably provide enablement for achieving sufficient isolation by passive components (i.e., RD) and active circuitry (i.e., together; See Claims 1 and 10). The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make the invention commensurate in scope with these claims. The Examiner doubts why the claimed invention needs "passive components" and "active circuitry" for achieving sufficient isolation because the specification states "alternatively, active circuitry such as transistors and operational amplifiers may be used instead of passive components to achieve isolation" on page 11, lines 25-27.

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claim 4 and 9 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

6. The term "approximately" in claim 4 is a relative term which renders the claim indefinite. The term "approximately" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. In this case, the claim 4 recites the subject matter "a value in a range of approximately 1 K Ω to 25 K Ω ". However, the term "approximately" in the claim makes the claims indefinite because no one could define the values of "approximately 1 K Ω to 25 K Ω ".

7. A broad range or limitation together with a narrow range or limitation that falls within the broad range or limitation (in the same claim) is considered indefinite, since the resulting claim does not clearly set forth the metes and bounds of the patent protection desired. Note the explanation given by the Board of Patent Appeals and Interferences in *Ex parte Wu*, 10 USPQ2d 2031, 2033 (Bd. Pat. App. & Inter. 1989), as to where broad language is followed by "such as" and then narrow language. The Board stated that this can render a claim indefinite by raising a question or doubt as to whether the feature introduced by such language is (a) merely exemplary of the remainder of the claim, and therefore not required, or (b) a required feature of the claims. Note also, for example, the decisions of *Ex parte Steigewald*, 131 USPQ 74 (Bd. App. 1961); *Ex parte Hall*, 83 USPQ 38 (Bd. App. 1948); and *Ex parte Hasche*, 86 USPQ 481 (Bd. App. 1949).

In the present instance, claim 9 recites the broad recitation "the isolation circuitry comprises passive components", and the claim also recites "the isolation circuitry having an impedance RD" on its parent claim, which is the narrower statement of the range/limitation. In fact, the Applicants define RD as an inline resistor (See Application, page 2, lines 20-22), which is a passive circuitry. However, the Applicants recite the broader limitation "the isolation circuitry comprises passive components" in the claim 9 since the subject matter "passive components" could be interpreted as an LC circuitry in addition to the resistor circuitry.

Claim Rejections - 35 USC § 103

8. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

9. Claims 12, 14 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takekuma et al. [US 5,568,063 A; hereinafter Takekuma] in view of Feldbaumer [US 5,382,841 A] and what was well known in the art, as exemplified by Matsuoka et al. [US 6,297,663 B1; Matsuoka].

Referring to claim 12, Takekuma discloses a common bus (i.e., transmission bus 100 of Fig. 11) comprising a signal line (i.e., transmission bus line) having first terminal (i.e., left-most connection point on transmission line 100 for terminal resistor 50 in Fig. 11) of an associated first current limiting element (i.e., termination resistors 50 and 51 in Fig. 11) d.c. coupled to a first supply level (See col. 7, lines 10-13), said first current limiting element of impedance RA (i.e., each termination resistor has 50 Ω ; See col. 7, lines 10-11); isolation circuitry (i.e., resistors 80-83 in Fig. 11) electrically coupling each of said signal line of said common bus to a plurality of electronic devices (i.e., circuit blocks 1-4 in Fig. 11; See col. 7, lines 1-7), each device having a corresponding signal line to enable communication of signals between said common bus and said plurality of electronic devices (See col. 1, lines 33+).

Takekuma does not teach switching circuitry for signal line of said common bus, wherein said switching circuitry selectively couples a second terminal of said associated first current limiting element to a second supply level to select a logic level of said associated signal line.

Feldbaumer discloses a switchable active bus termination circuit (Fig. 1), wherein said bus termination circuit comprising switching circuitry (i.e., switching circuit 18 of Fig. 1) for signal line of a common bus (i.e., electrical conductor 21 of Fig. 1), wherein said switching circuitry selectively couples a second terminal (i.e., connection point on terminal resistor 20 for switching circuit 18 in Fig. 1) of an associated first current limiting element (i.e., resistor 20 of Fig. 1) to a second supply level to select a logic level of said associated signal line (See col. 2, lines 54-65).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said switchable active bus termination circuit, as disclosed by Feldbaumer, in said apparatus, as disclosed by Takekuma, so as to reduce signal reflections with said passive resistor termination being inherent drift and inaccuracies of setting resistor values (See Feldbaumer, col. 1, lines 38-47 and col. 4, lines 19-22).

Takekuma, as modified by Feldbaumer, does not expressly teach said common bus comprising a plurality of said signal lines, and each said device having corresponding said plurality of signal lines.

The Examiner takes Official Notice that (1) a bus system has a bus constructed of a plurality of signal lines, and (2) even though only one bit line of bus is illustrated in Fig. 11 of Takekuma and Fig. 1 of Feldbaumer, practically, circuit configurations each having the construction in those figures are arranged in parallel by the number corresponding to a bit width of bus, is well known to one of ordinary skill in the art, as evidenced by Matsuoka in Abstract and at col. 4, lines 9-12.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have included a plurality of signal lines in said common bus since it would allow each said device to have corresponding said plurality of signal lines to enable communication of said signals between said common bus and said plurality of electronic devices.

Referring to claim 14, Takekuma teaches said isolation circuitry (i.e., resistors 80-83 in Fig. 11) is passive isolation circuitry (in fact, resistor component is a passive component).

Referring to claim 18, Takekuma teaches RA for each selected signal line of said common bus is selected to have a value of 50Ω (i.e., value in a range of 10Ω to $5K\Omega$; See col. 7, lines 8-13).

Furthermore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have set up said impedance RA in a range of 10Ω to $5K\Omega$, since it has been held that where the general conditions of a claim are disclosed in the prior art (See Takekuma, col. 7, lines 1-7)

discovering the optimum or workable range involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

10. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takekuma [US 5,568,063 A] in view of Feldbaumer [US 5,382,841 A] as applied to claims 12, 14 and 18 above, and further in view of Graham [US 4,445,048].

Referring to claim 13, Takekuma, as modified by Feldbaumer, discloses all the limitations of the claim 13 except that does not expressly teach a plurality of connectors for removably coupling said plurality of signal lines of each electronic device to said corresponding plurality of signal lines of said common bus through said isolation circuitry.

Graham discloses a high speed ribbon cable bus (i.e., ribbon cable 10 of Fig. 4), wherein a plurality of connectors (i.e., connectors 23 in Fig. 3) for removably coupling a plurality of signal lines (See col. 5, lines 5-14) of each electronic device (i.e., unit A, B, C in Fig. 1) to a corresponding plurality of signal lines (i.e., leads 11a, 11b, 12a, 12b, ... 13a, 13b in Fig. 1) of a common bus (i.e., ribbon cable bus 10 of Fig. 1) through an isolation circuitry (i.e., trough resistors 32 in Fig. 3).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have implemented said common bus, as disclosed by Takekuma, as modified by Feldbaumer, in said high speed ribbon cable bus, as disclosed by Graham, for the advantage of reducing cost of said common bus (See Graham, col. 1, lines 19-22).

11. Claims 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takekuma [US 5,568,063 A] in view of Feldbaumer [US 5,382,841 A] as applied to claims 12, 14 and 18 above, and further in view of Graham [US 4,445,048] and what was well known in the art, as exemplified by Pemberton [US 5,564,024 A].

Referring to claim 15, Takekuma teaches said isolation circuitry (i.e., resistors 80-83 in Fig. 11) is a resistor of impedance RD in a range of 10 Ω to 100 Ω (See col. 7, lines 45-51).

Takekuma, as modified by Feldbaumer, is silent that said range is 1 K Ω to 25 K Ω .

However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have set up said impedance RD in a range of 1 K Ω to 25 K Ω , since it has been held that where the general conditions of a claim are disclosed in the prior art, such that said impedance RD of said resistor may be calculated by $R_m = Z_s - Z_0 / 2$, wherein Z_s denotes an impedance of transmission line, Z_0 denotes an impedance of said signal line, and R_m denotes a resistance of said isolation circuitry (See Takekuma, col. 8, lines 50-55), discovering the optimum or workable range involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

Takekuma, as modified by Feldbaumer, still does not expressly teach said isolation circuitry is an inline resistor.

The Examiner takes Official Notice that said isolation circuitry could be implemented in an inline resistor, is well known to one of ordinary skill in the art, as evidenced by Pemberton at col. 2, lines 56-60, wherein in fact that SCSI device termination is typically supplied via a number of single in-line packages which are socketed to a circuit board associated with the internal device implies said isolation circuitry (i.e., similar structure to the SCSI termination structure) could be implemented in an inline resistor (i.e., single in-line package resistor) which are socketed to said corresponding plurality of signal lines of said electronic device.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have implemented said isolation circuitry in said inline resistor since it would provide a convenient way to substitute said isolation circuitry in case of repairing/testing/diagnostic services.

Referring to claim 16, Takekuma teaches said isolation circuitry (i.e., resistors 80-83 in Fig. 11) is an in-line resistor of impedance RD in conjunction with a pull up resistor (i.e., resistors 80-83 in conjunction with termination resistors 50 and 51 in Fig. 11), wherein RD in a range of 10 Ω to 100 Ω (i.e., less than 1 K Ω ; See col. 7, lines 45-51).

12. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takekuma [US 5,568,063 A] in view of Feldbaumer [US 5,382,841 A] as applied to claims 12, 14 and 18 above, and further in view of Wigger [US 6,011,710 A].

Referring to claim 17, Takekuma, as modified by Feldbaumer, discloses all the limitations of the claim 17 except that does not expressly teach said isolation circuitry is active isolation circuitry.

Wiggers discloses a capacitance reducing memory system (See Abstract), wherein an isolation circuitry (i.e., switches 29 in Fig. 4; See col. 5, lines 14-19) is active isolation circuitry (i.e., FET type switches; See col. 4, lines 53-60).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted said passive type isolation circuitry (i.e., resistors), as disclosed by Takekuma, as modified by Feldbaumer, by said active type isolation circuitry (i.e., FET type switches 29 in Fig. 4), as disclosed by Wiggers, for the advantage of allowing said backplane apparatus (i.e., memory system) configuration to be easily changed by simply adding said electronic devices (i.e., modules) or by replacing some or all of said electronic devices (See Wiggers, col. 4, lines 61-65).

13. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takekuma [US 5,568,063 A] in view of Feldbaumer [US 5,382,841 A] as applied to claims 12, 14 and 18 above, and further in view of what was well known in the art, as exemplified by Fisher et al. [US 5,572,685 A; hereinafter Fisher].

Referring to claim 20, Takekuma, as modified by Feldbaumer, discloses all the limitations of the claim 20 except that does not expressly teach said electronic device is a disk drive.

The Examiner takes Official Notice that said electronic device being a disk drive, is well known to one of ordinary skill in the art, as evidenced by Fisher (See Fig. 1 and col. 3, lines 15-32).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have included said disk drive in said backplane apparatus as said electronics device since it would provide a large capacity of non-volatile memory array.

Allowable Subject Matter

14. Claims 1-3, 5, 7 and 11 are allowed.

15. The following is a statement of reasons for the indication of allowable subject matter:

The limitations of claim 1 are deemed allowable over the prior art of record as the prior art fails to teach or suggest that the isolation circuitry having an impedance RD, wherein (impedance of said current limiting element RA + impedance of said isolation circuitry RD) $\geq 3.3K\Omega$, wherein RD $\leq 25K\Omega$. The claims 2-3, 5, 7 and 11 are the dependent claims of the claim 1.

16. Claims 4 and 9 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Response to Arguments

17. Applicants' arguments with respect to the response to the claims rejection under 35 U.S.C. 103(a) have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

18. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

With regard to Modular Bus Structure,

Dillon et al. [US 5,663,661] disclose modular bus with single or double parallel termination.

With regard to Bus System,

Sanwo et al. [US 5,019,728] disclose high speed CMOS backpanel transceiver.

Shimizu et al. [US 5,046,072] disclose signal distribution system.

Williams [US 6,222,389 B1] discloses assisted gunning transceiver logic (AGTL) bus driver.

With regard to Bus Cabling,

Daly et al. [US 5,955,703 A] disclose circuitized electrical cable and method of assembling same.

Los et al. [US 5,620,331 A] disclose feed-thru IDC terminator.

19. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher E. Lee whose telephone number is 703-305-5950. The examiner can normally be reached on 9:00am - 5:00pm.

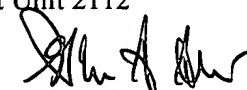
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

cel/



Christopher E. Lee
Examiner
Art Unit 2112



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Primary Patent Examiner
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